

S/N 08/903,486

PATENTIN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant: Leonard Forbes et al.

Examiner:

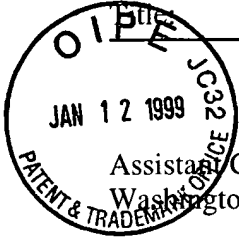
Serial No.: 08/903,486

Group Art Unit: 2812

Filed: July 29, 1997

Docket: 303.326US1

SILICON CARBIDE GATE TRANSISTOR AND FABRICATION PROCESS


 Assistant Commissioner for Patents
 Washington, D.C. 20231
SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT
 I.D.S
 #2 1/2
 2-20-99
 T. Flower

In compliance with the duty imposed by 37 C.F.R. § 1.56, and in accordance with 37 C.F.R. §§ 1.97 *et. seq.*, the enclosed materials are brought to the attention of the Examiner for consideration in connection with the above-identified patent application. Applicants respectfully request that this Information Disclosure Statement be entered and the documents listed on the attached Form 1449 be considered by the Examiner and made of record. Pursuant to the provisions of MPEP 609, Applicants further request that a copy of the 1449 form, initialled by the Examiner to indicate that all listed citations have been considered, be returned with the next official communication.

Under 37 C.F.R. § 1.97(b)(3), it is believed that no fee or certificate is required with this Information Disclosure Statement. However, if an Office Action on the merits has been mailed, the Commissioner is hereby authorized to charge any additional fees or credit any overpayment to Account No. 19-0743.

The Examiner is invited to contact the Applicants' Representative at the below-listed telephone number if there are any questions regarding this communication.

Respectfully submitted,

RECEIVED

LEONARD FORBES ET AL.

JAN 15 1999

By their Representatives,

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Date

Jan 6, 1999

By

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I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to Assistant Commissioner of Patents, Washington, D.C. 20231 on January 6, 1999.

Name

Daniel J. Kluth

Signature

Daniel J. Kluth